WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

at least one input element; and

a protective circuit coupled to the input element, the protective circuit operable to protect the integrated circuit from electrostatic discharge, the protective circuit comprising:

a lateral NPN transistor coupled to the input element, and operable to activate when the input element voltage exceeds a threshold, the threshold greater than or equal to the ordinary operating voltage of circuitry coupled to the input element; and

a lateral PNP transistor coupled to the input element and to the lateral NPN transistor, the lateral PNP transistor operable to aid in raising a potential of the base of the lateral NPN transistor.

2. The integrated circuit of Claim 1 wherein the collector of the lateral PNP transistor is connected to the base of the lateral NPN transistor.

3. The integrated circuit of Claim 1 wherein the lateral PNP transistor comprises the drain, source and channel region of a p-channel MOSFET.

4. The protective circuit of Claim 1 wherein the protective circuit further comprises a vertical PNP operable to aid in raising the potential of the base of the lateral NPN transistor, the vertical PNP transistor coupled to the lateral NPN transistor and to the input element.

5. The integrated circuit of Claim 1 wherein the lateral NPN transistor comprises a plurality of lateral NPN transistors connected in parallel, and surrounded by a substrate biasing area.

6. The integrated circuit of Claim 1 wherein the lateral NPN transistor comprises a plurality of lateral NPN transistors in parallel, each of the plurality located near a positively-doped diffusion in the substrate.

7. The integrated circuit of Claim 1 wherein the lateral NPN transistor comprises a plurality of lateral NPN transistors in parallel, each of the plurality located within approximately five microns of a positively-doped diffusion in the substrate.

8. A protective circuit for electrostatic discharge protection, comprising:

a lateral NPN transistor operable to couple to an input element, the lateral NPN transistor further operable to activate when the input element voltage exceeds a threshold, the threshold greater than or equal to the ordinary operating voltage of circuitry coupled to the input element; and

a lateral PNP transistor operable to couple to the input element and to the lateral NPN transistor, the lateral PNP transistor operable to aid in raising a potential of the base of the lateral NPN transistor.

9. The protective circuit of Claim 8 wherein the collector of the lateral PNP transistor is connected to the base of the lateral NPN transistor.

10. The protective circuit of Claim 8 wherein the lateral PNP transistor comprises the drain, source and channel region of a p-channel MOSFET.

11. The protective circuit of Claim 8 wherein the protective circuit further comprises a vertical PNP operable to aid in raising the potential of the base of the lateral NPN transistor, the vertical PNP transistor operable to couple to the lateral NPN transistor and to the input element.

12. The protective circuit of Claim 8 wherein the lateral NPN transistor comprises a plurality of lateral NPN transistors connected in parallel and surrounded by a substrate biasing area.

13. The protective circuit of Claim 8 wherein the lateral NPN transistor comprises a plurality of lateral NPN transistors in parallel, ones of the plurality including a positively-doped diffusion in the substrate between them.

14. The protective circuit of Claim 8 wherein the lateral NPN transistor comprises a plurality of lateral NPN transistors in parallel, each of the plurality located within approximately five microns of a positively-doped diffusion in the substrate.

15. A method for providing electrostatic discharge protection, comprising:

coupling internal circuitry of an integrated circuit to an input element;

coupling to the input element a lateral NPN transistor operable to activate when the input element voltage exceeds a threshold, the threshold greater than or equal to the ordinary operating voltage of the internal circuitry; and

coupling to the input element, the internal circuitry of the integrated circuit, and the lateral NPN transistor a lateral PNP transistor operable to aid in raising a potential of the base of the lateral NPN transistor.

16. The method of Claim 15 wherein the collector of the lateral PNP transistor is connected to the base of the lateral NPN transistor.

17. The method of Claim 15 wherein the lateral PNP transistor comprises the drain, source and channel region of a p-channel MOSFET.

18. The method of Claim 15 wherein the lateral NPN transistor comprises a plurality of lateral NPN transistors connected in parallel, and surrounded by a substrate biasing area.

19. The method of Claim 15 wherein the lateral NPN transistor comprises a plurality of lateral NPN transistors in parallel, each of the plurality located near a positively-doped diffusion in the substrate.

20. The method of Claim 15 wherein the lateral NPN transistor comprises a plurality of lateral NPN transistors in parallel, each of the plurality located within approximately five microns of a positively-doped diffusion in the substrate.

21. An integrated circuit comprising:

at least one input element; and

a protective circuit coupled to the input element, the protective circuit operable to protect the integrated circuit from electrostatic discharge, the protective circuit comprising:

a lateral NPN transistor coupled to the input element, and operable to activate when the input element voltage exceeds a threshold, the threshold greater than or equal to the ordinary operating voltage of circuitry coupled to the input element; and

a PMOS transistor coupled to the input element and to the lateral NPN transistor, the PMOS transistor operable to aid in raising a potential of the base of the lateral NPN transistor.

22. The integrated circuit of Claim 21 wherein the n-well and the source of the PMOS transistor are connected to the input element, and the drain of the PMOS transistor is connected to the base of the lateral NPN transistor.

23. The integrated circuit of Claim 21 wherein the lateral NPN transistor comprises a plurality of lateral NPN transistors connected in parallel, and surrounded by a substrate biasing area.